

10 →

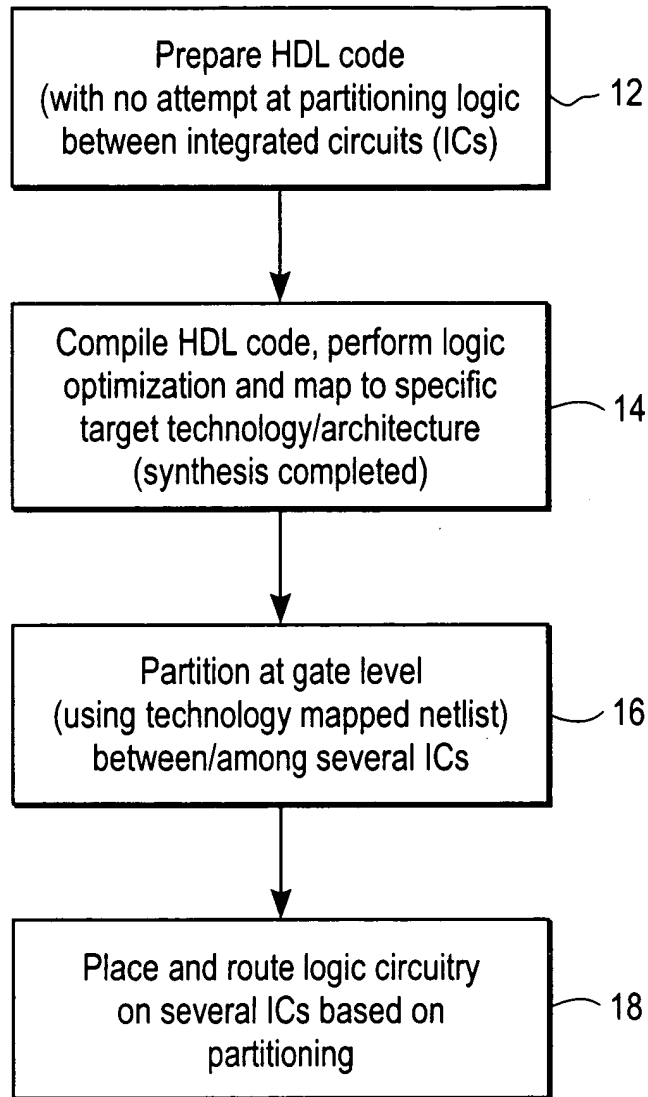


FIG. 1A (PRIOR ART)

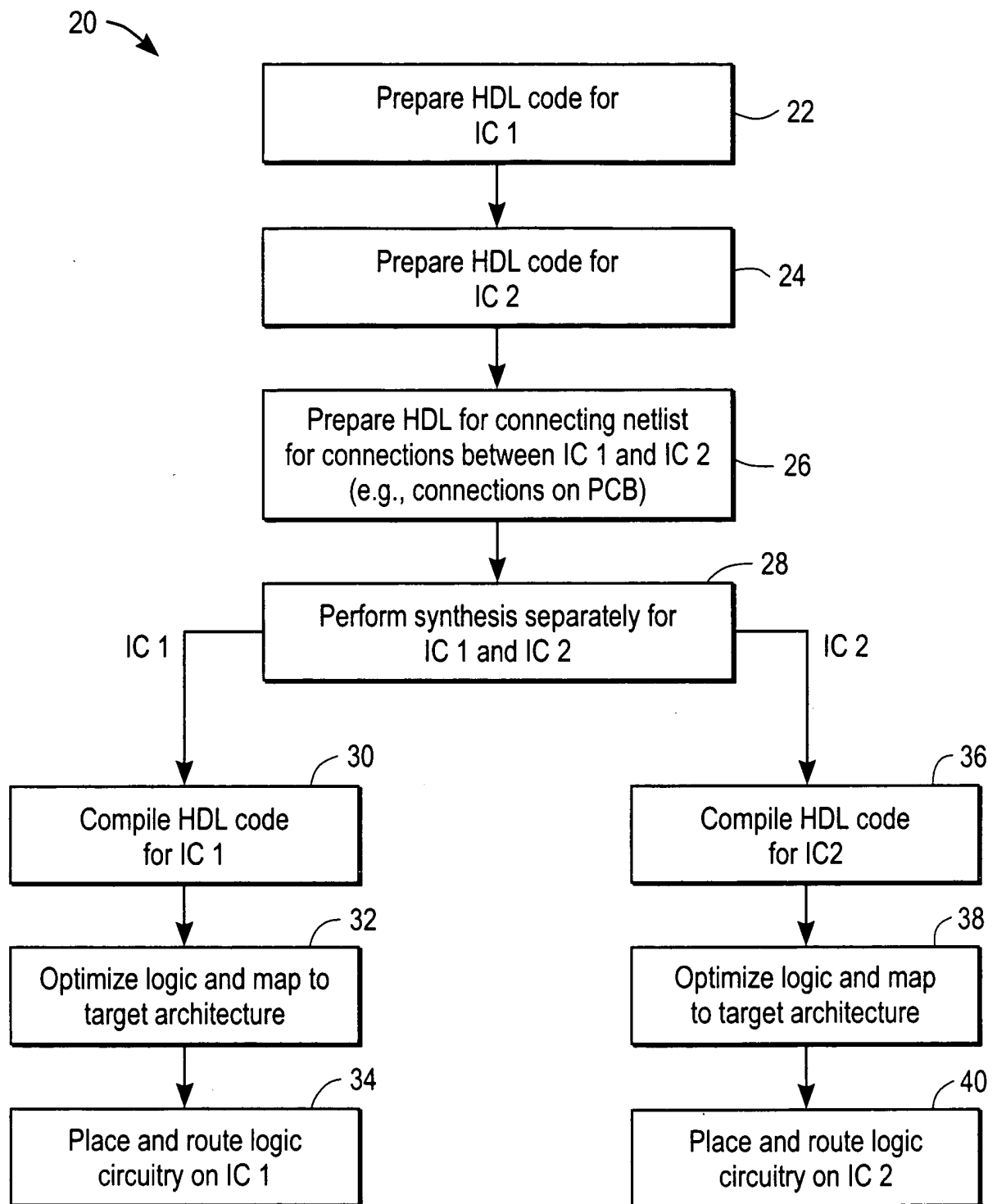


FIG. 1B (PRIOR ART)

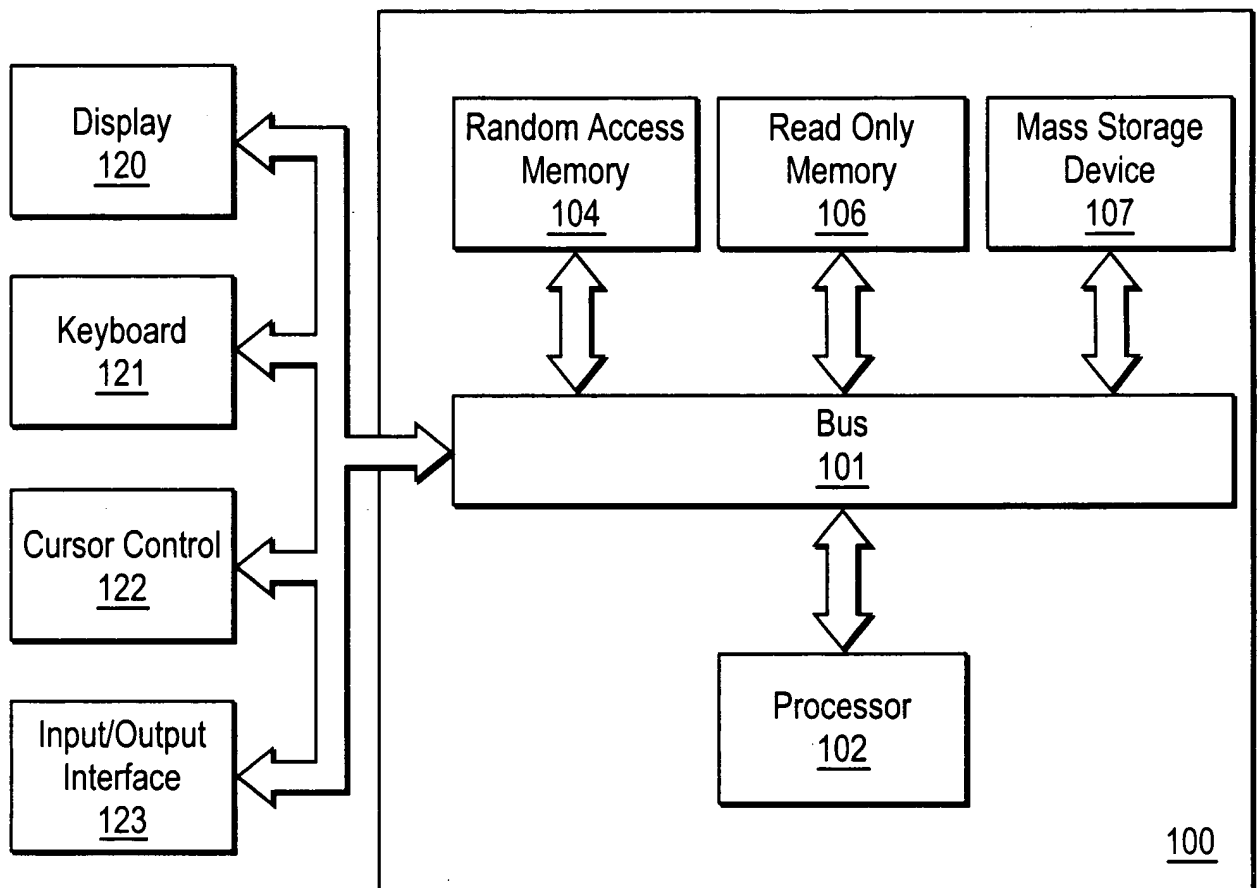


FIG. 2

201 →

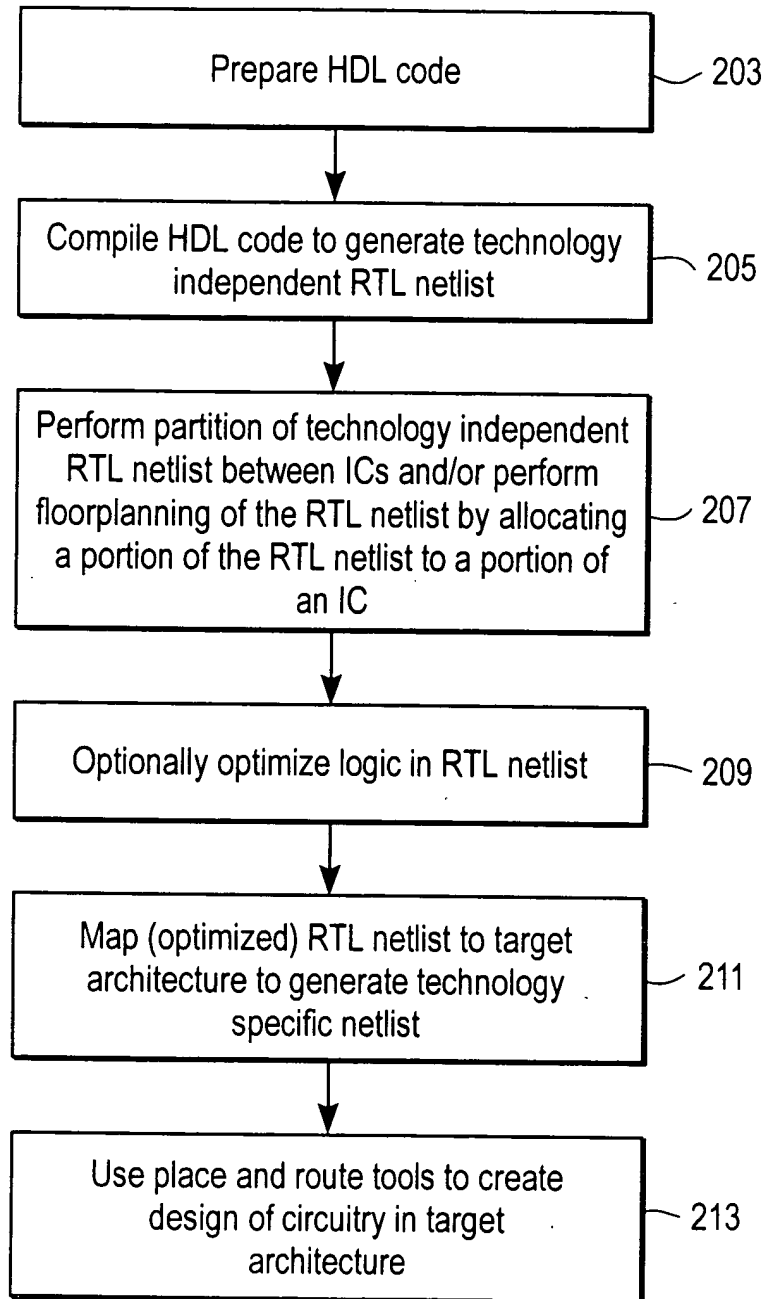


FIG. 3

301

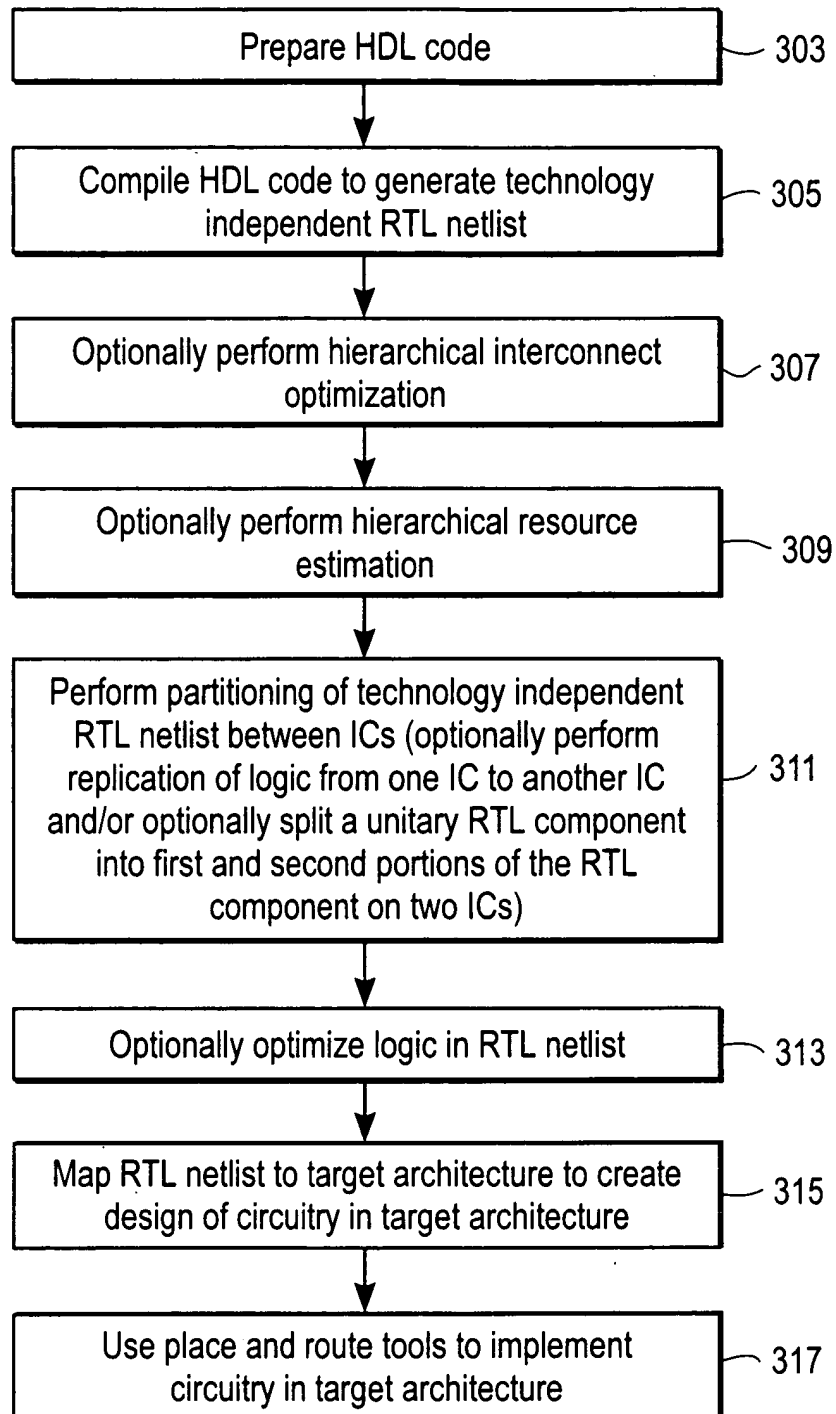


FIG. 4A

351

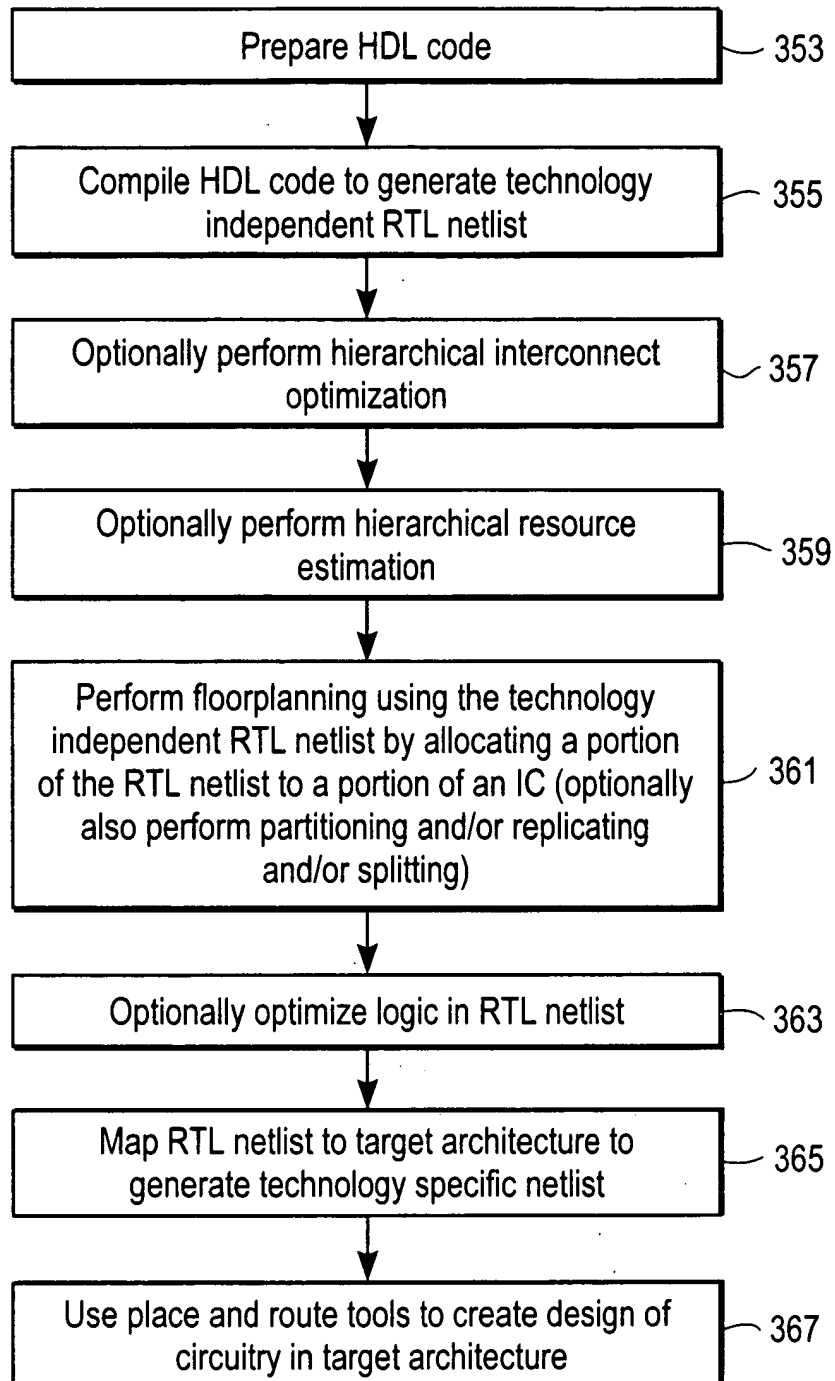


FIG. 4B

401

Hierarchical Interconnect Optimization

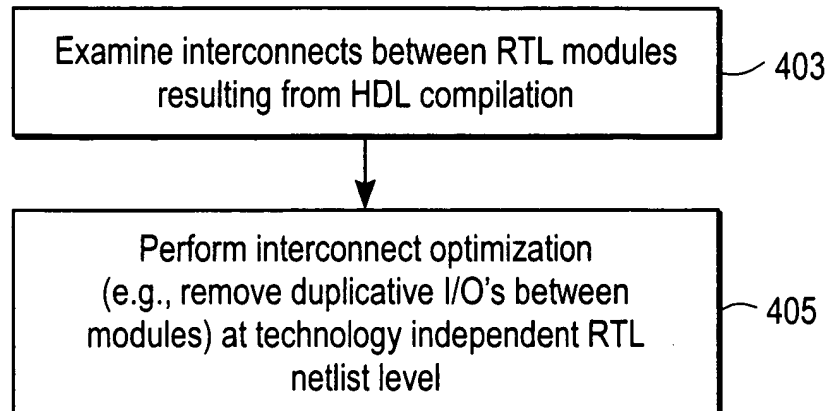


FIG. 5A

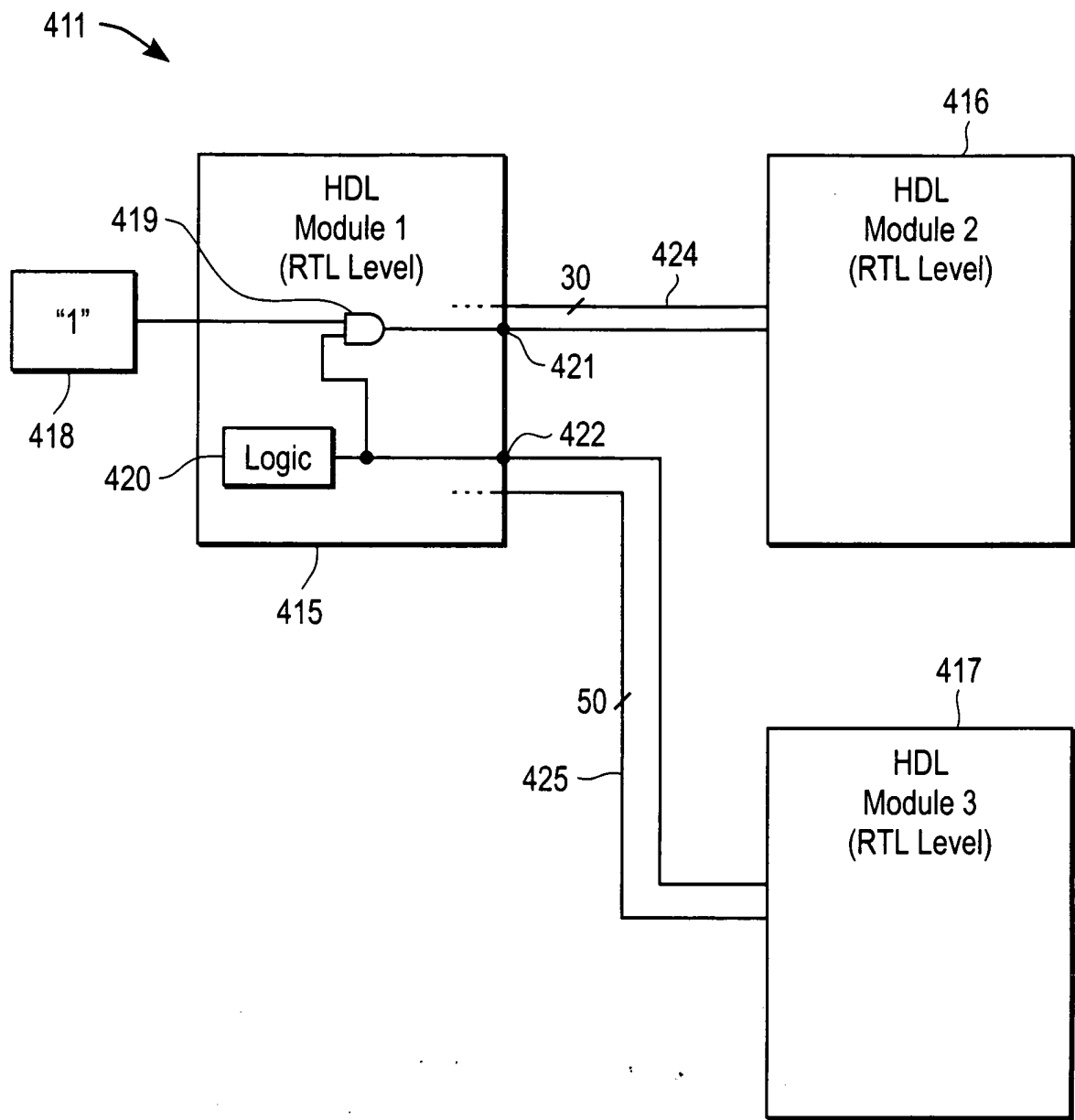


FIG. 5B

501

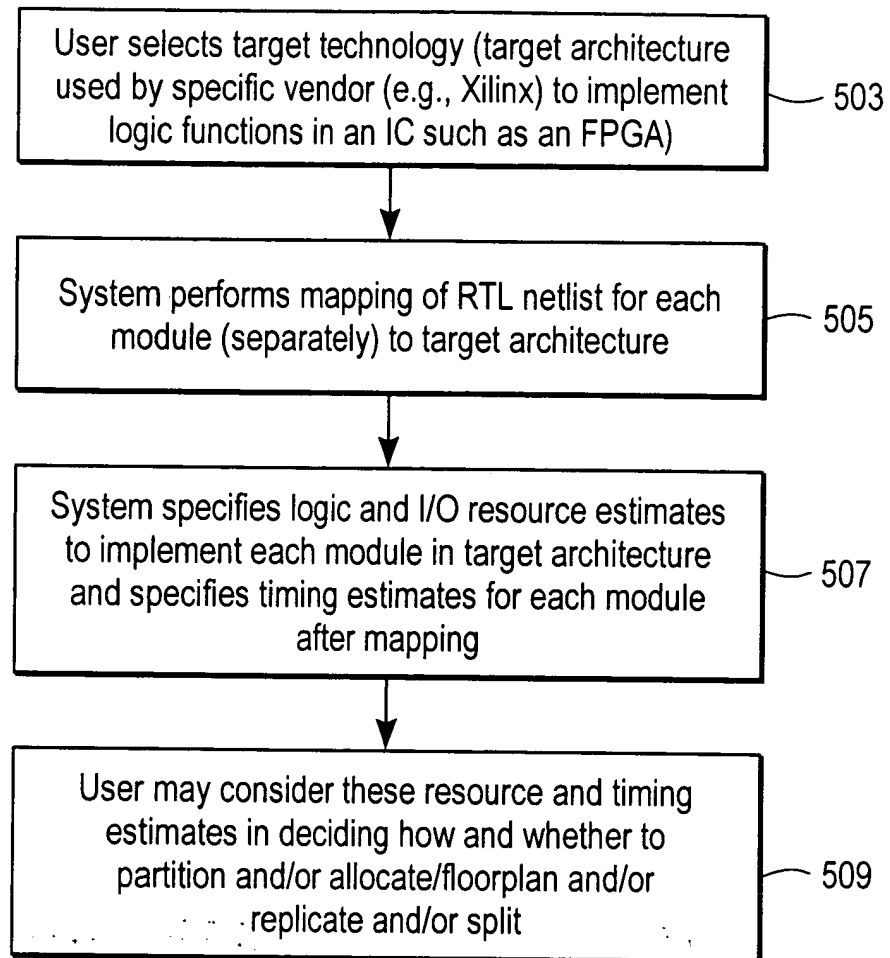


FIG. 6

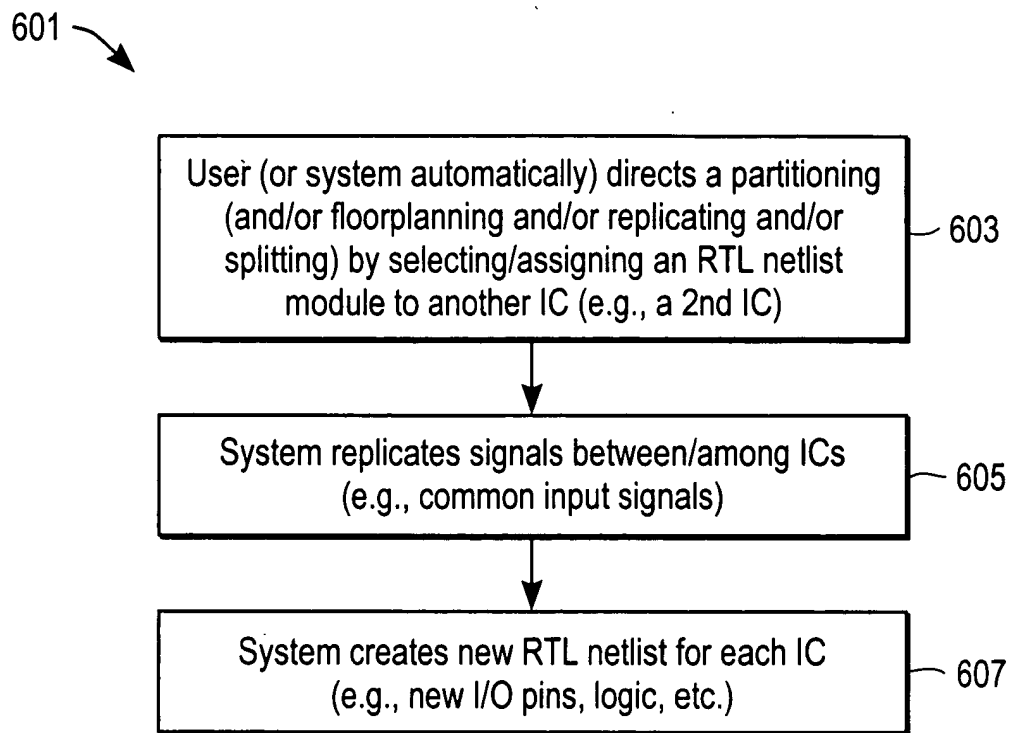


FIG. 7A

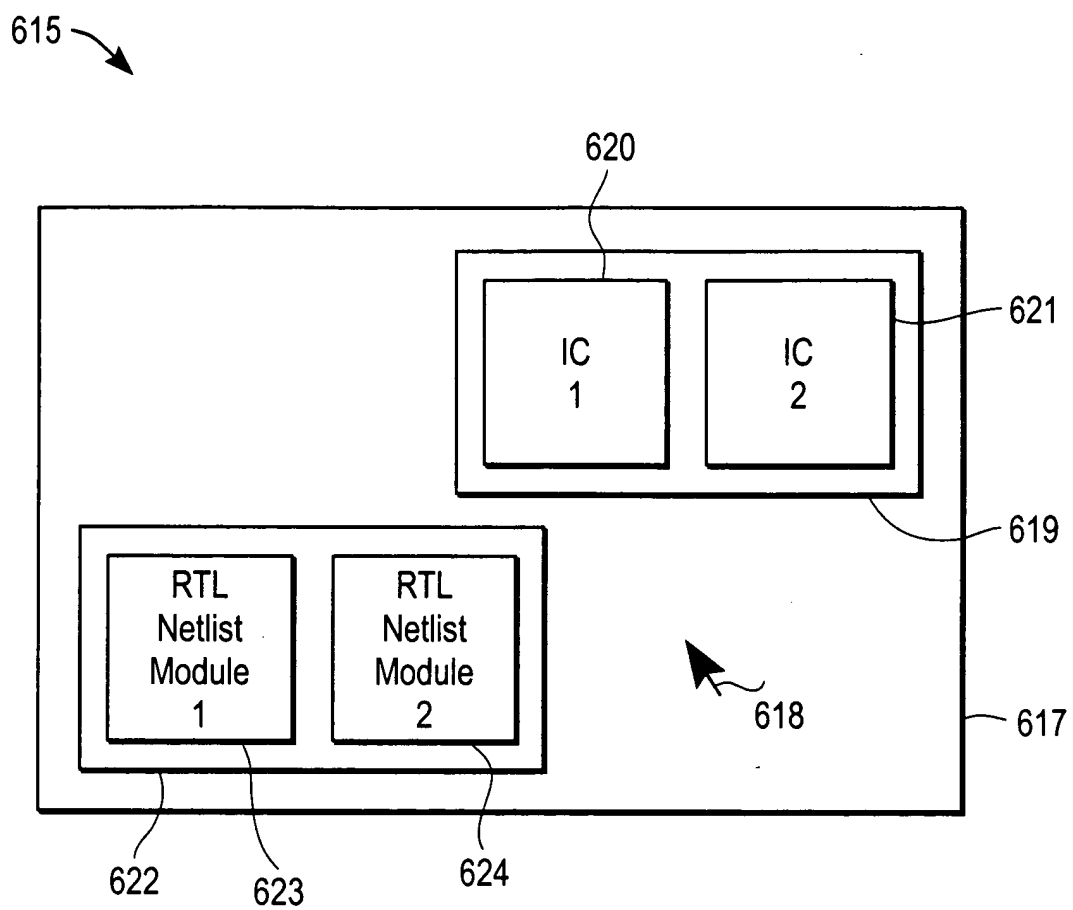


FIG. 7B

```

module prep2_2 (DATA0, DATA1, DATA2, LDPRE, SEL, RST, CLK, LDCOMP);
output [7:0] DATA0;
input [7:0] DATA1, DATA2;
input LDPRE, SEL, RST, CLK, LDCOMP;
    wire [7:0] DATA0_internal;
    prep2_1 inst1 (CLK, RST, SEL, LDCOMP, LDPRE, DATA1, DATA2, DATA0_internal);
    prep2_1 inst2 (CLK, RST, SEL, LDCOMP, LDPRE, DATA0_internal, DATA2, DATA0);
endmodule

```

703

```

module prep2_1 (CLK, RST, SEL, LDCOMP, LDPRE, DATA1, DATA2, DATA0);
input CLK, RST, SEL, LDCOMP, LDPRE;
input [7:0] DATA1, DATA2;
output [7:0] DATA0;
reg [7:0] DATA0;
reg [7:0] highreg_output, lowreg_output; // internal registers

wire compare_output = (DATA == lowreg_output); // comparator
wire [7:0] mux_output = SEL ? DATA1 : highreg_output; // mux

// registers
always @ (posedge CLK or posedge RST)
begin
    if (RST) begin
        highreg_output = 0;
        lowreg_output = 0;
    end else begin
        if (LDPRE)
            highreg_output = DATA2;
        if (LDCOMP)
            lowreg_output = DATA2;
    end
end

// counter
always @ (posedge CLK or posedge RST)
begin
    if (RST)
        DATA0 = 0
    else if (compare_output) // load
        DATA0 = mux_output;
    else
        DATA0 = DATA0 + 1;
end
endmodule

```

705

701

FIG. 8A

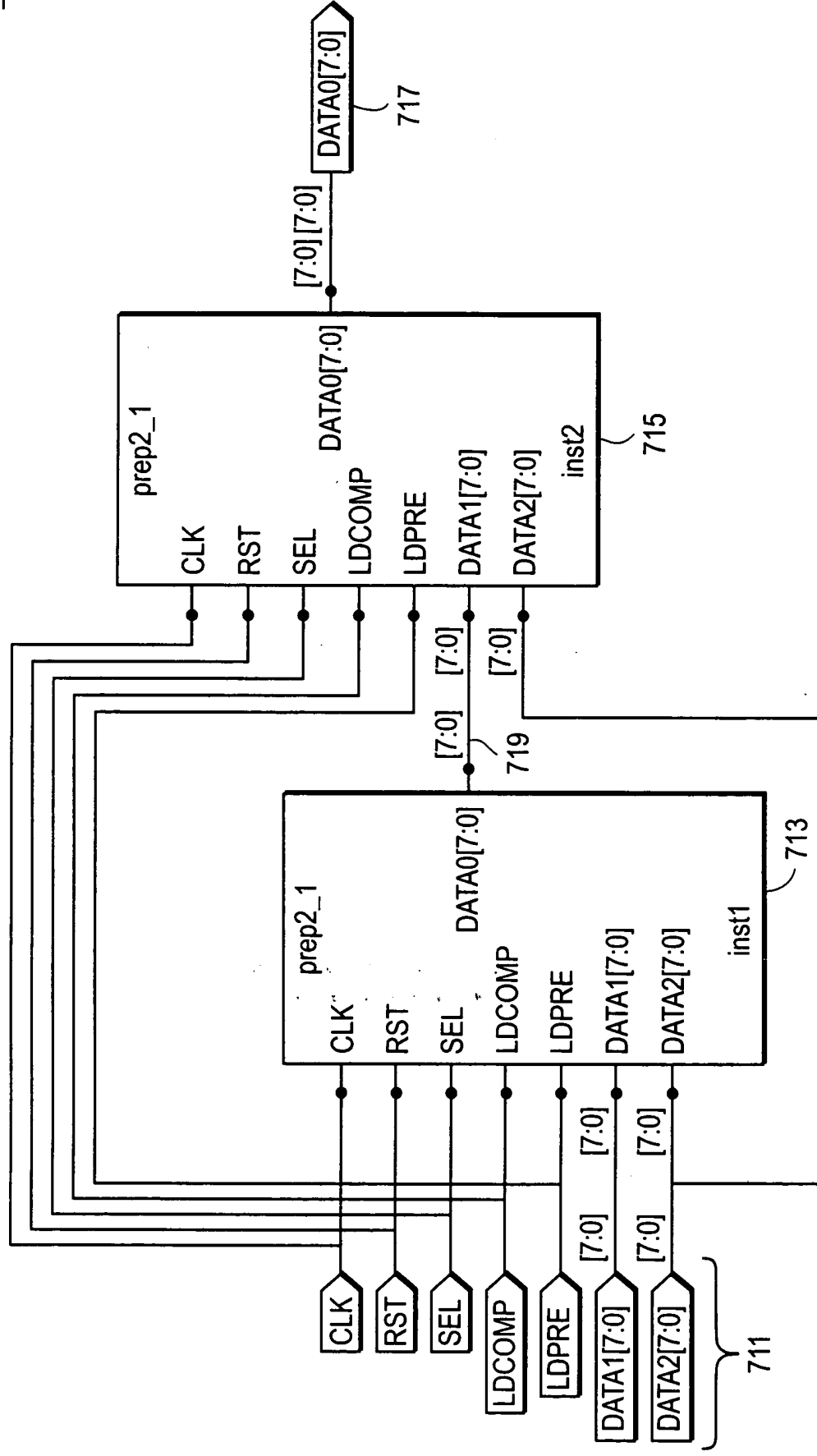
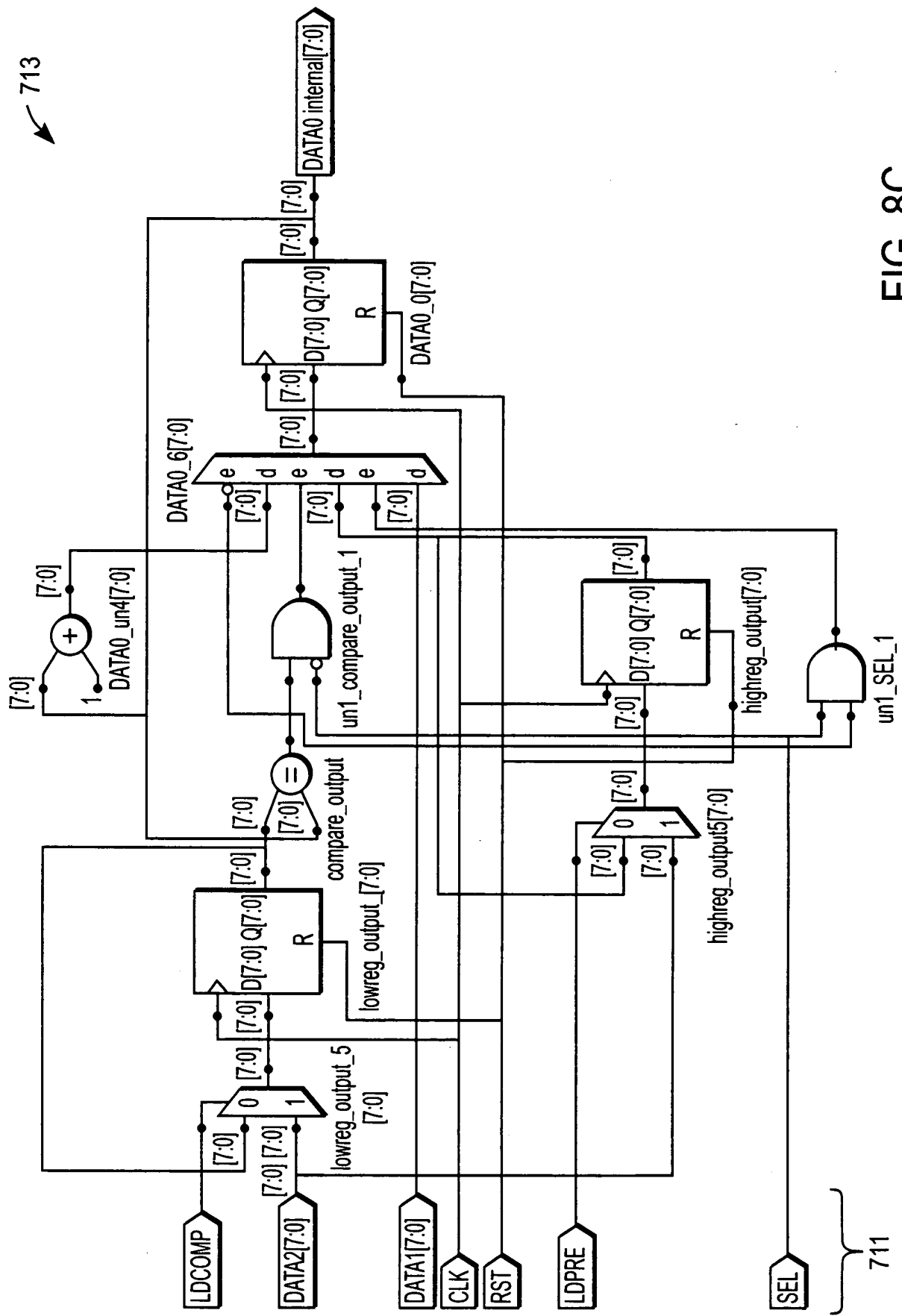


FIG. 8B



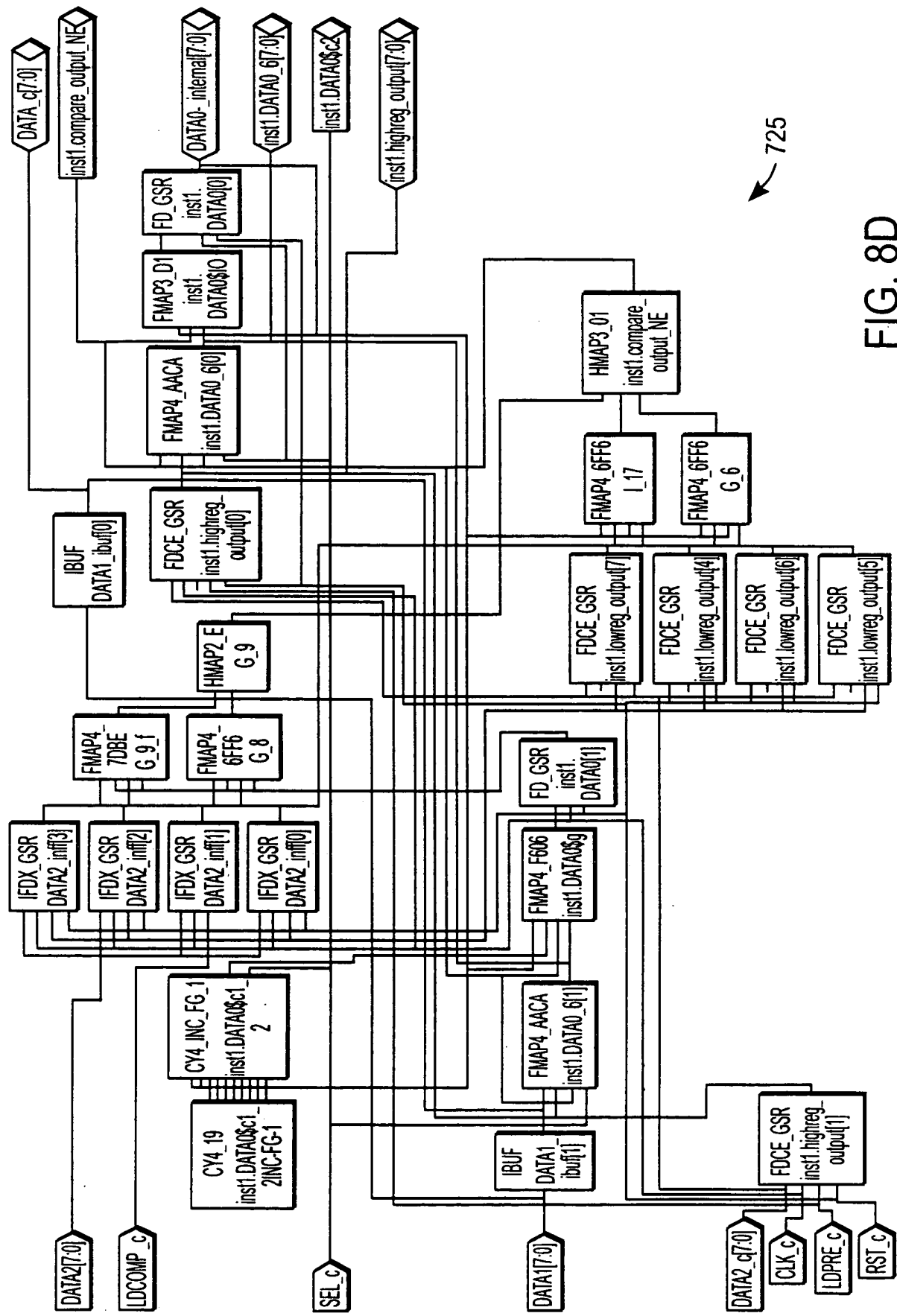


FIG. 8D

725

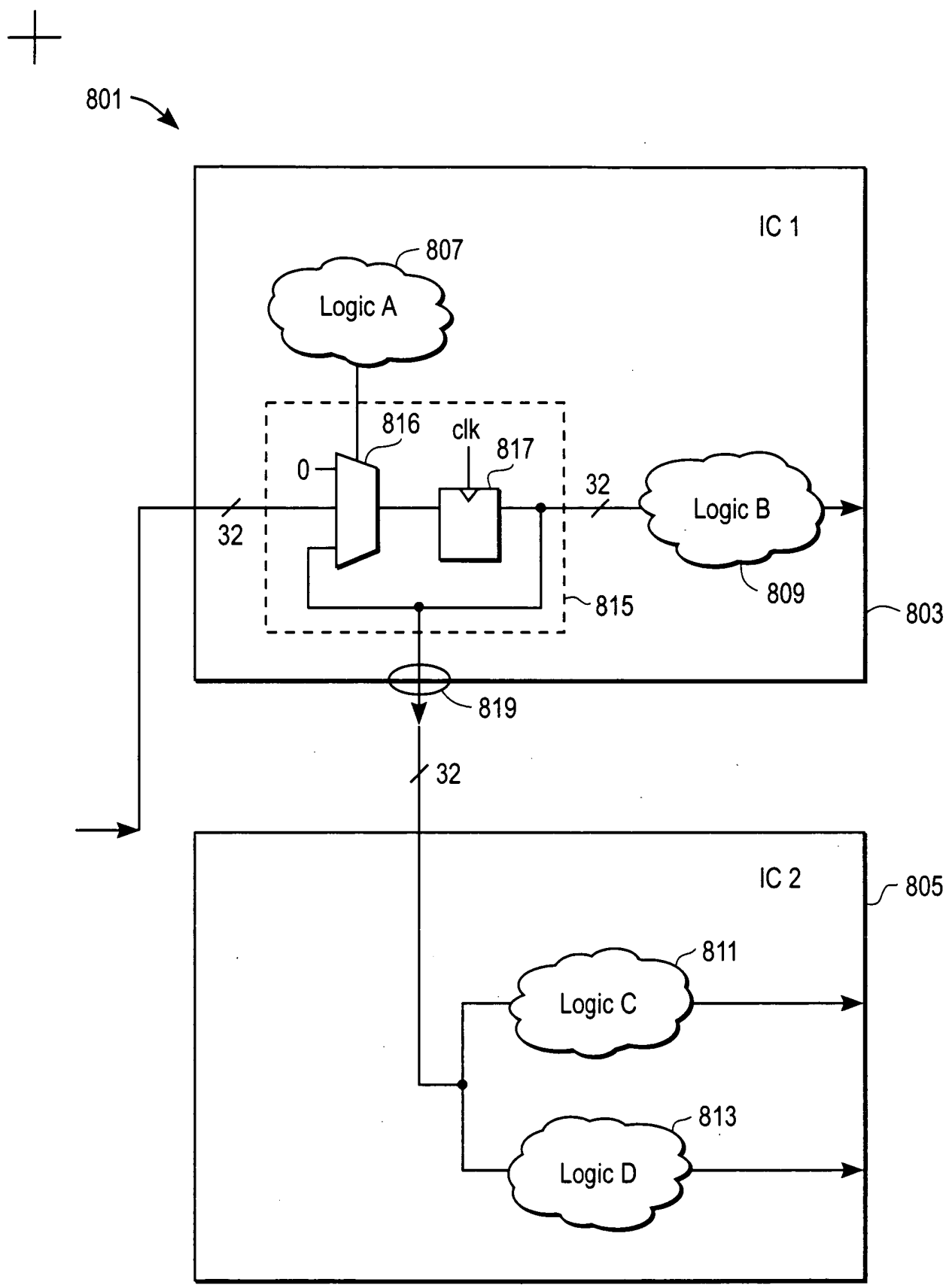


FIG. 9A



801A

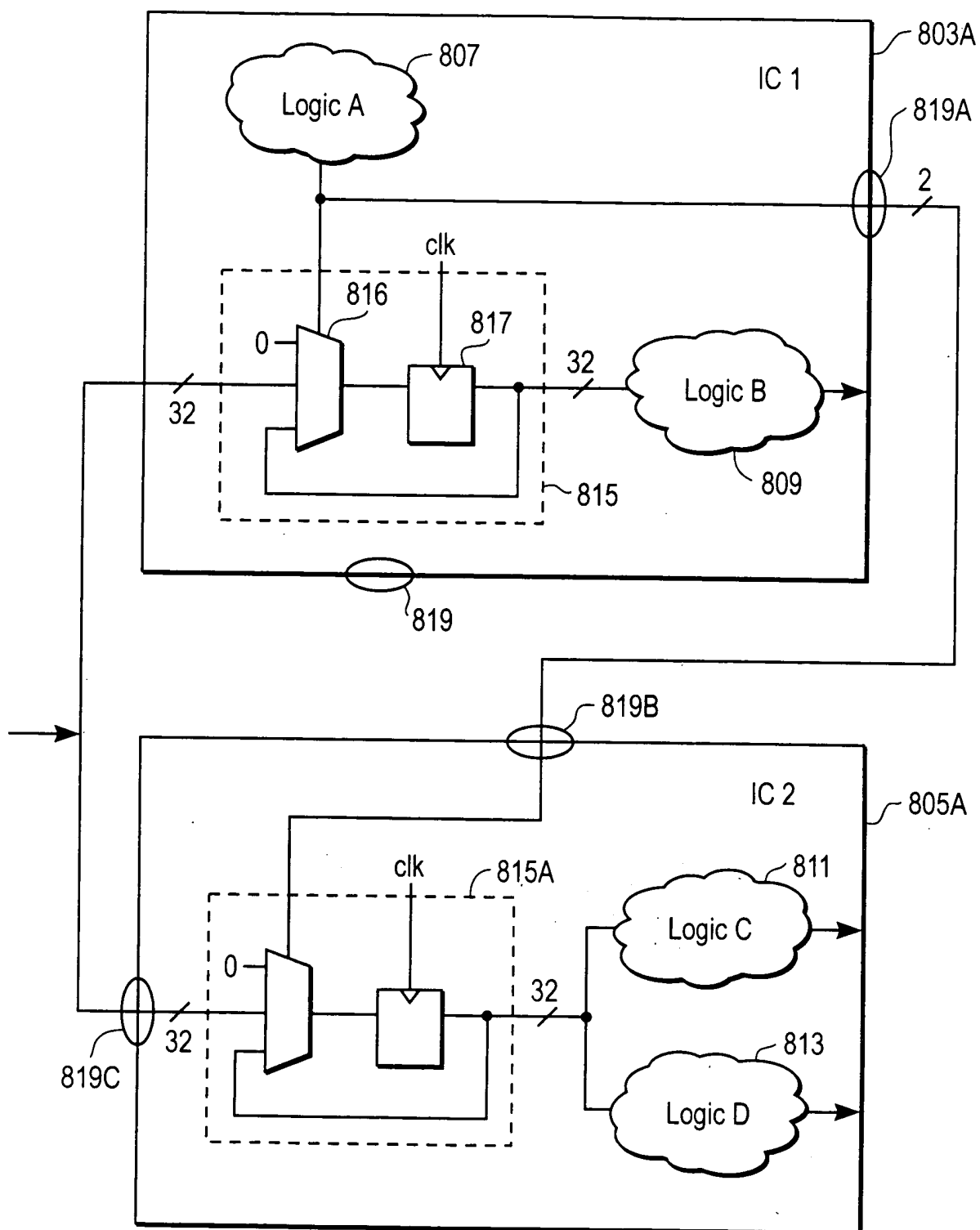


FIG. 9B



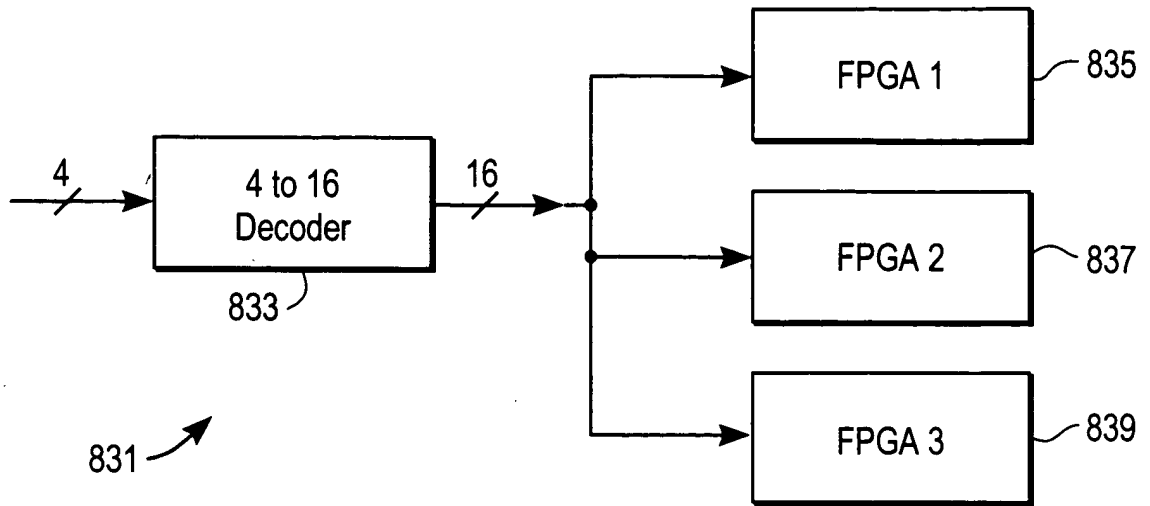


FIG. 9C

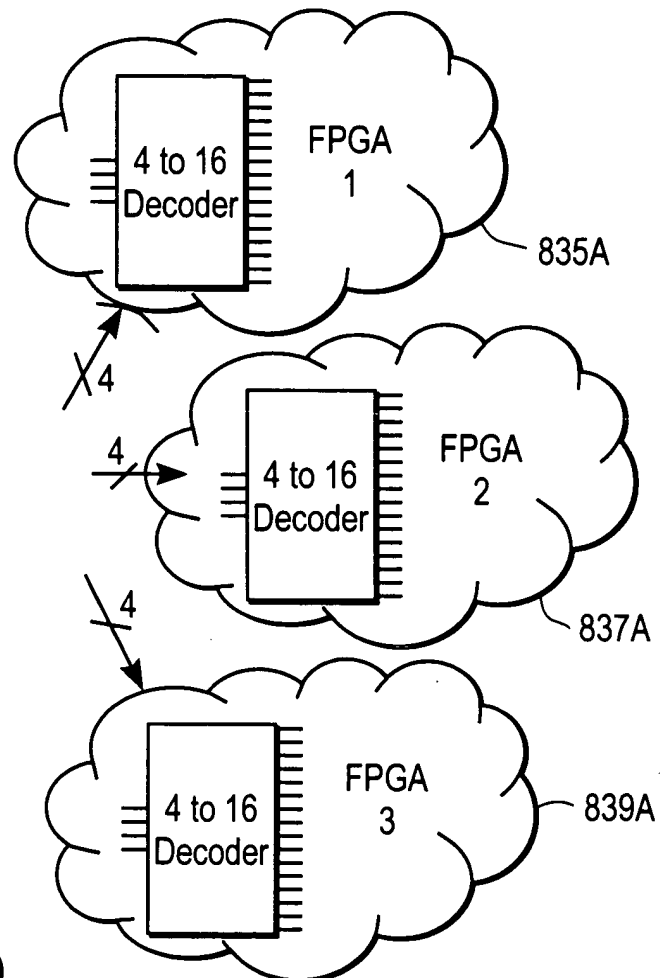


FIG. 9D



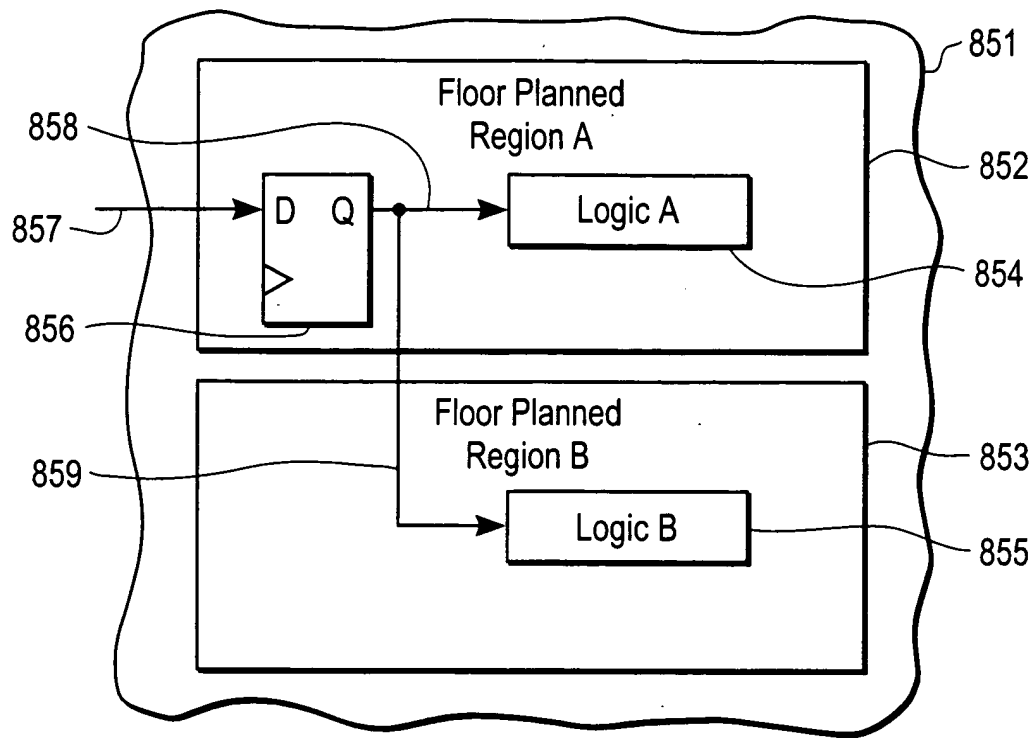


FIG. 9E

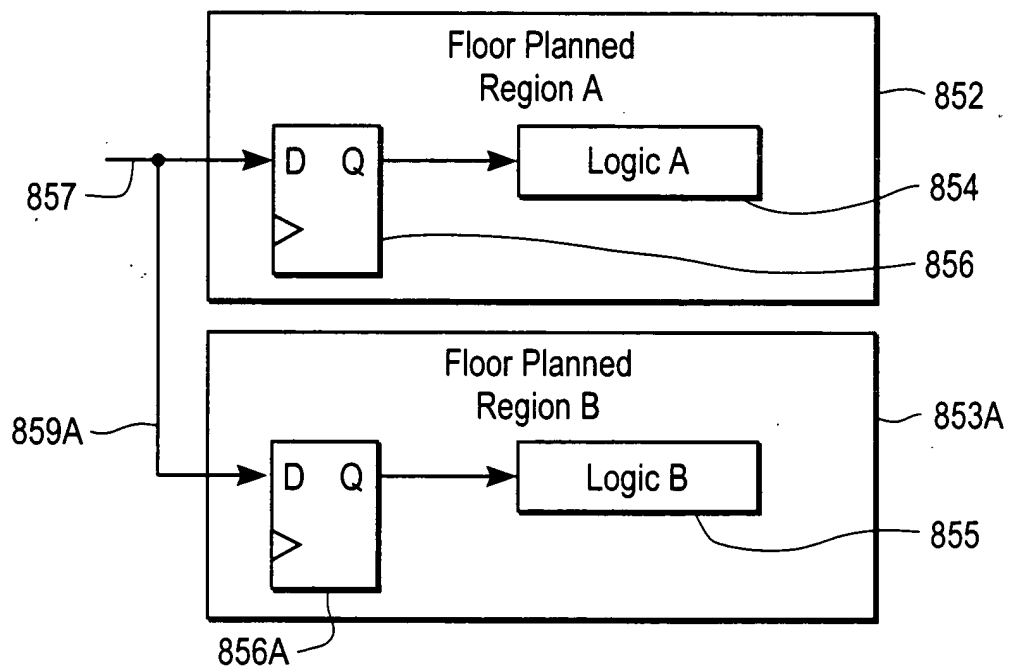


FIG. 9F

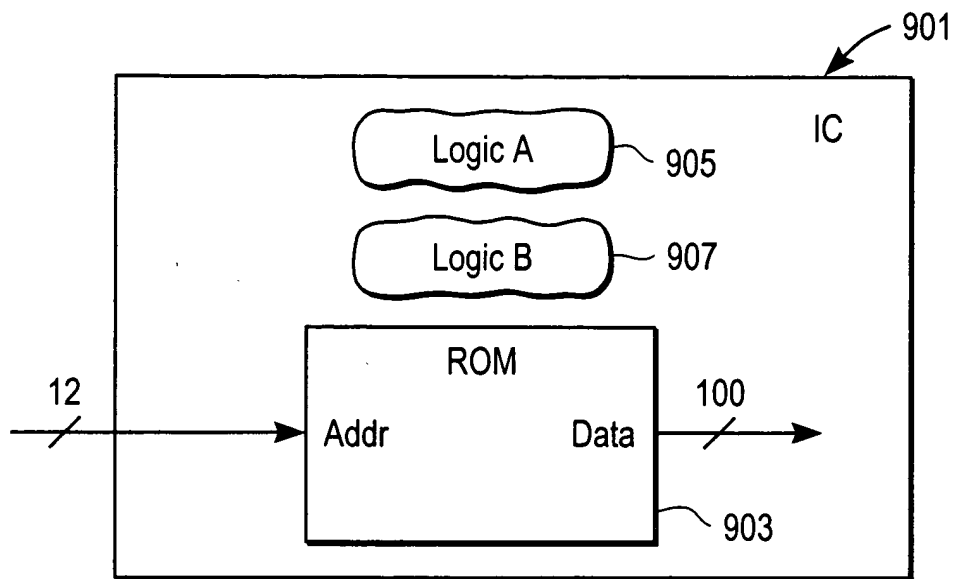


FIG. 10A

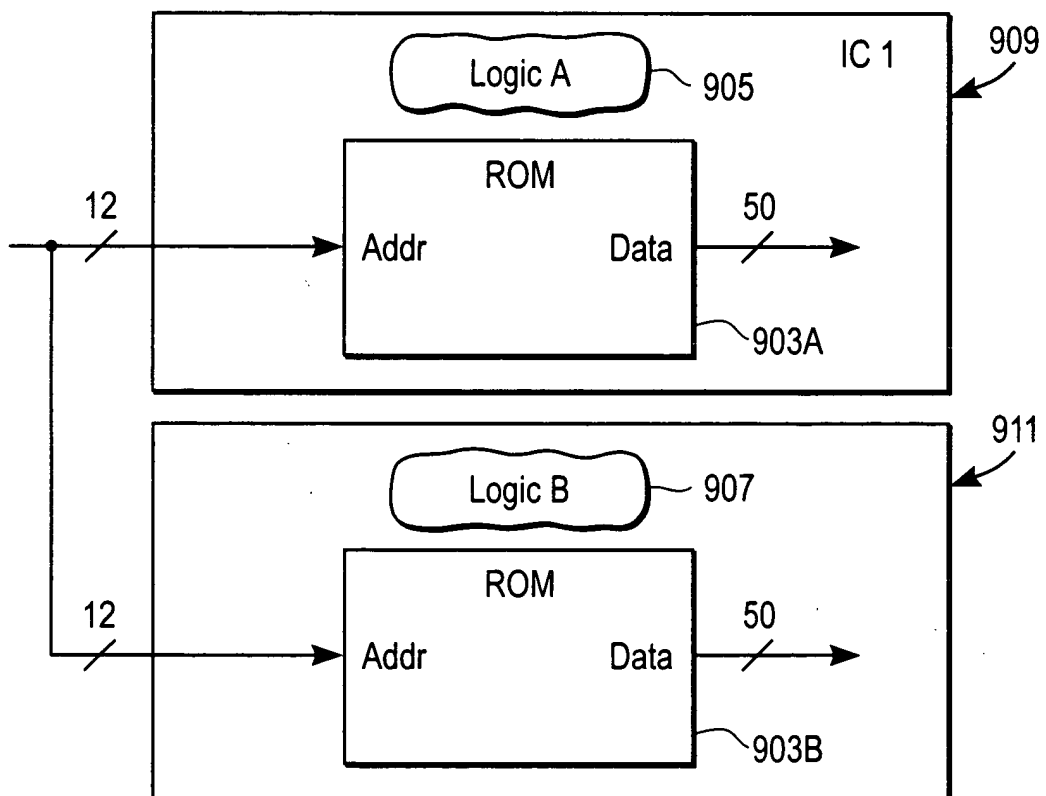


FIG. 10B

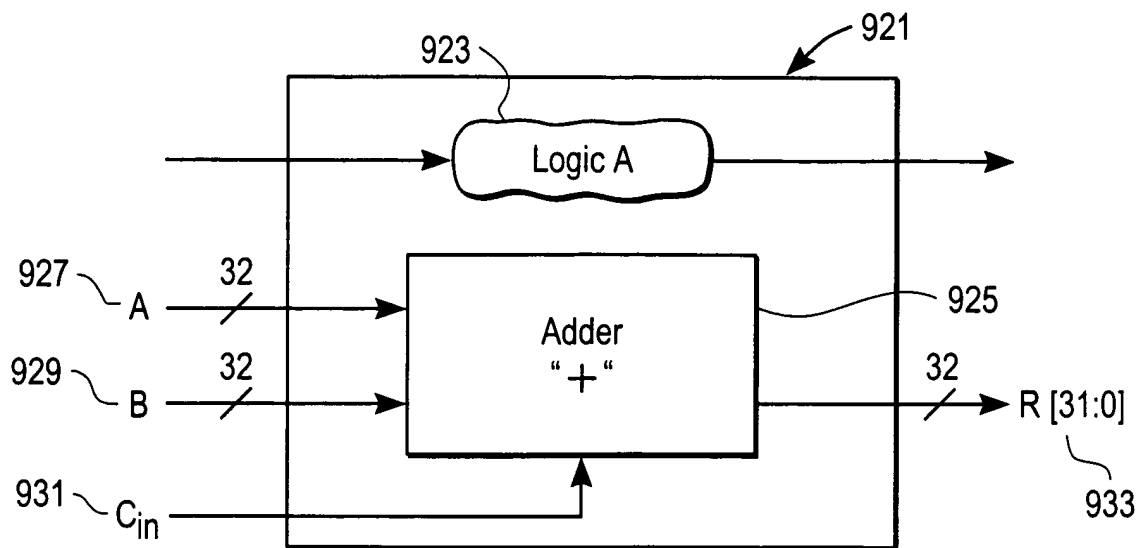


FIG. 10C

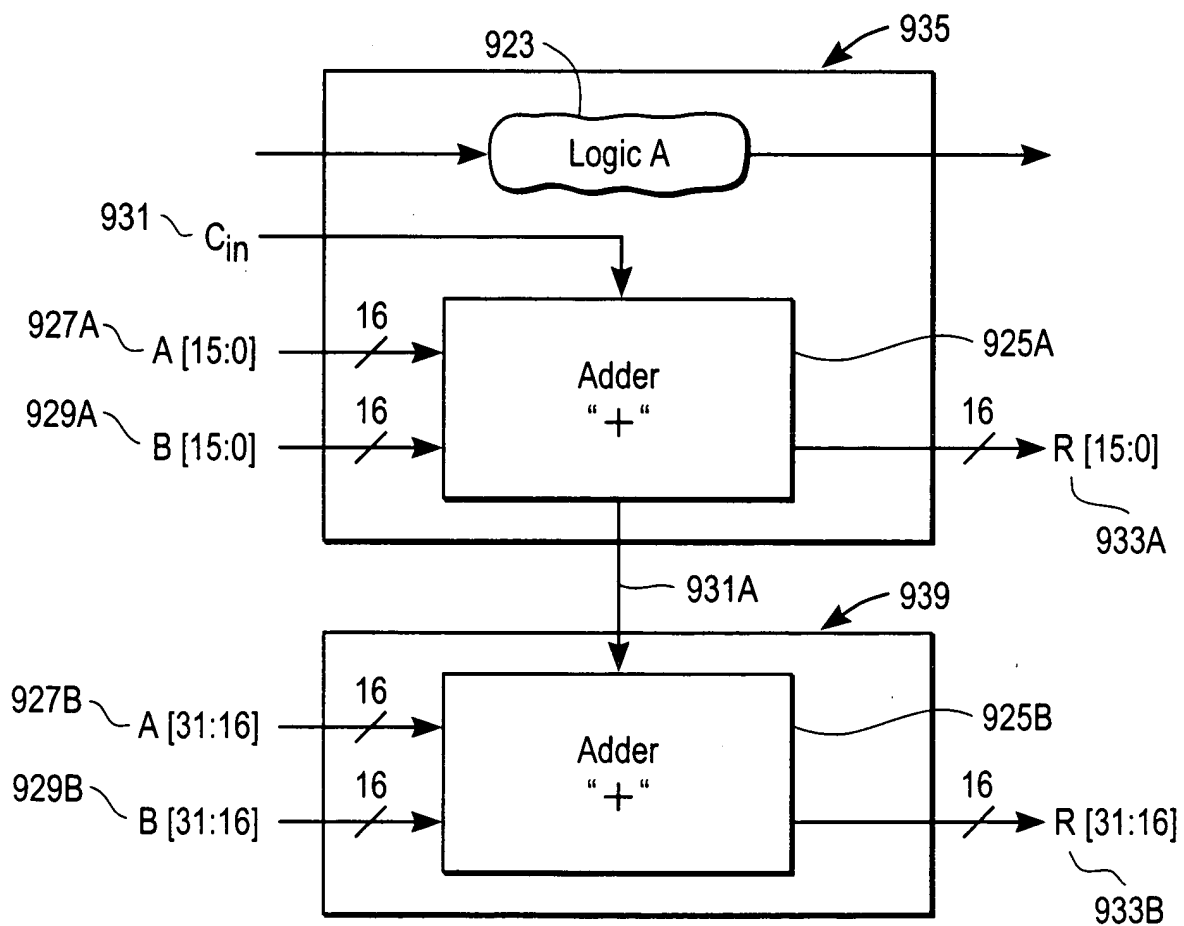


FIG. 10D



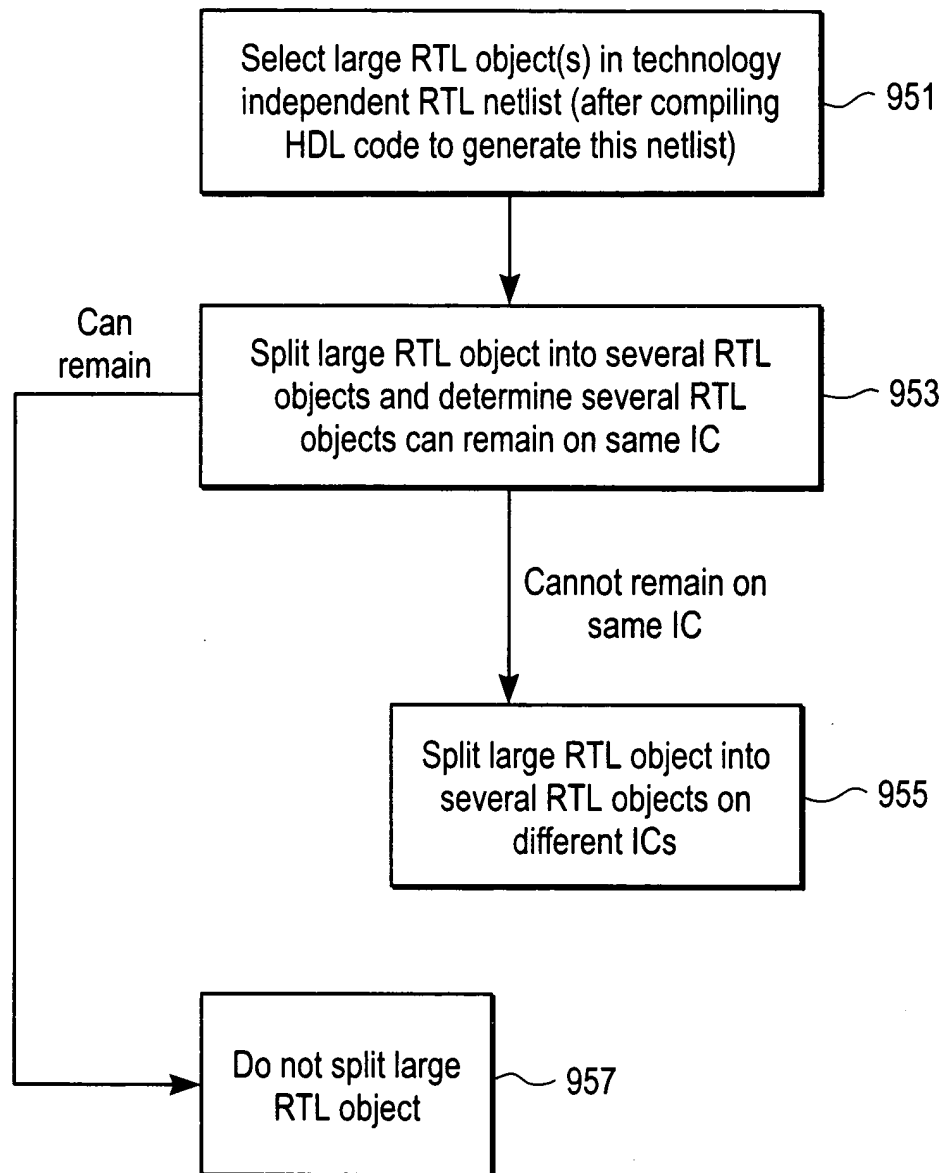


FIG. 10E

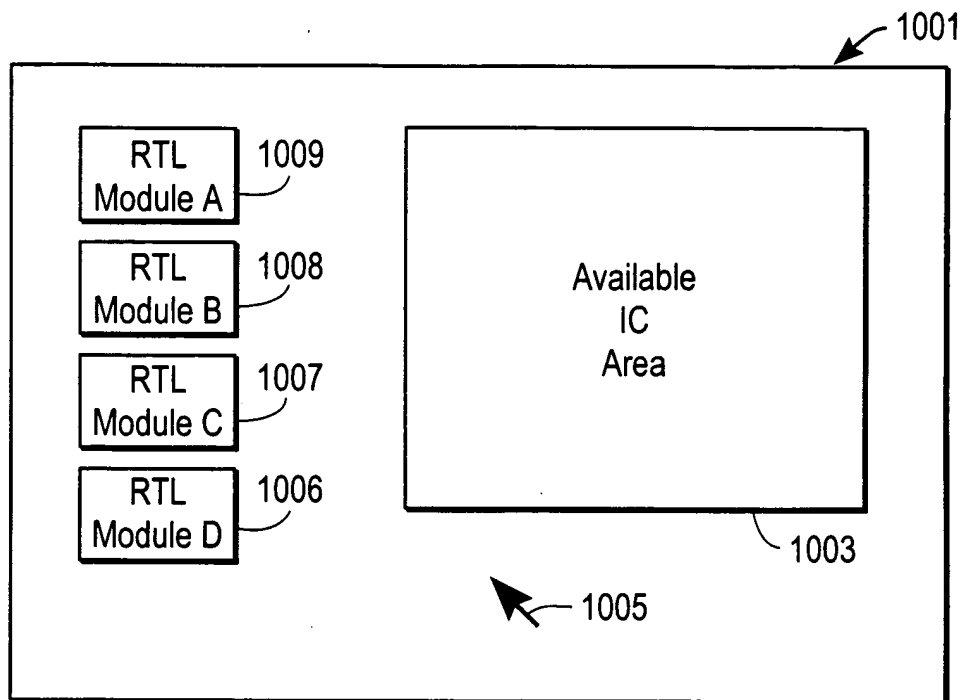


FIG. 11A

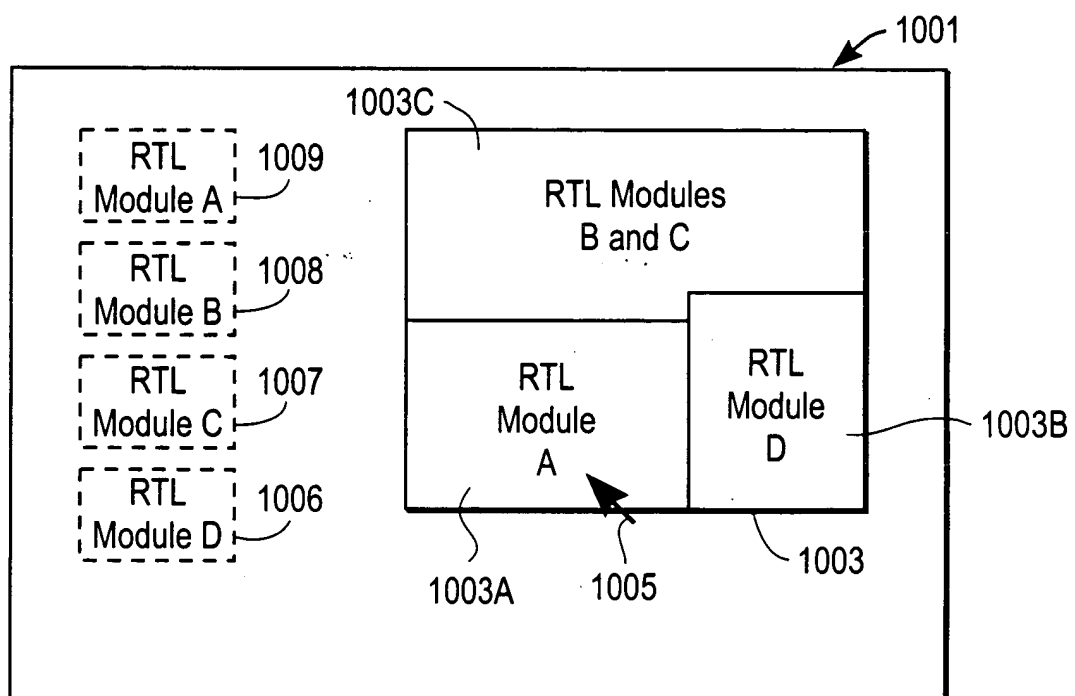


FIG. 11B

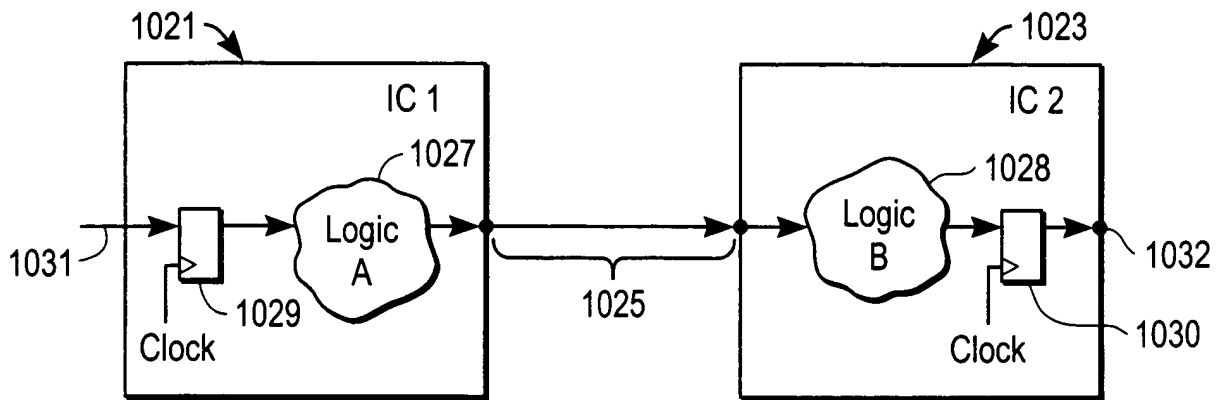


FIG. 12

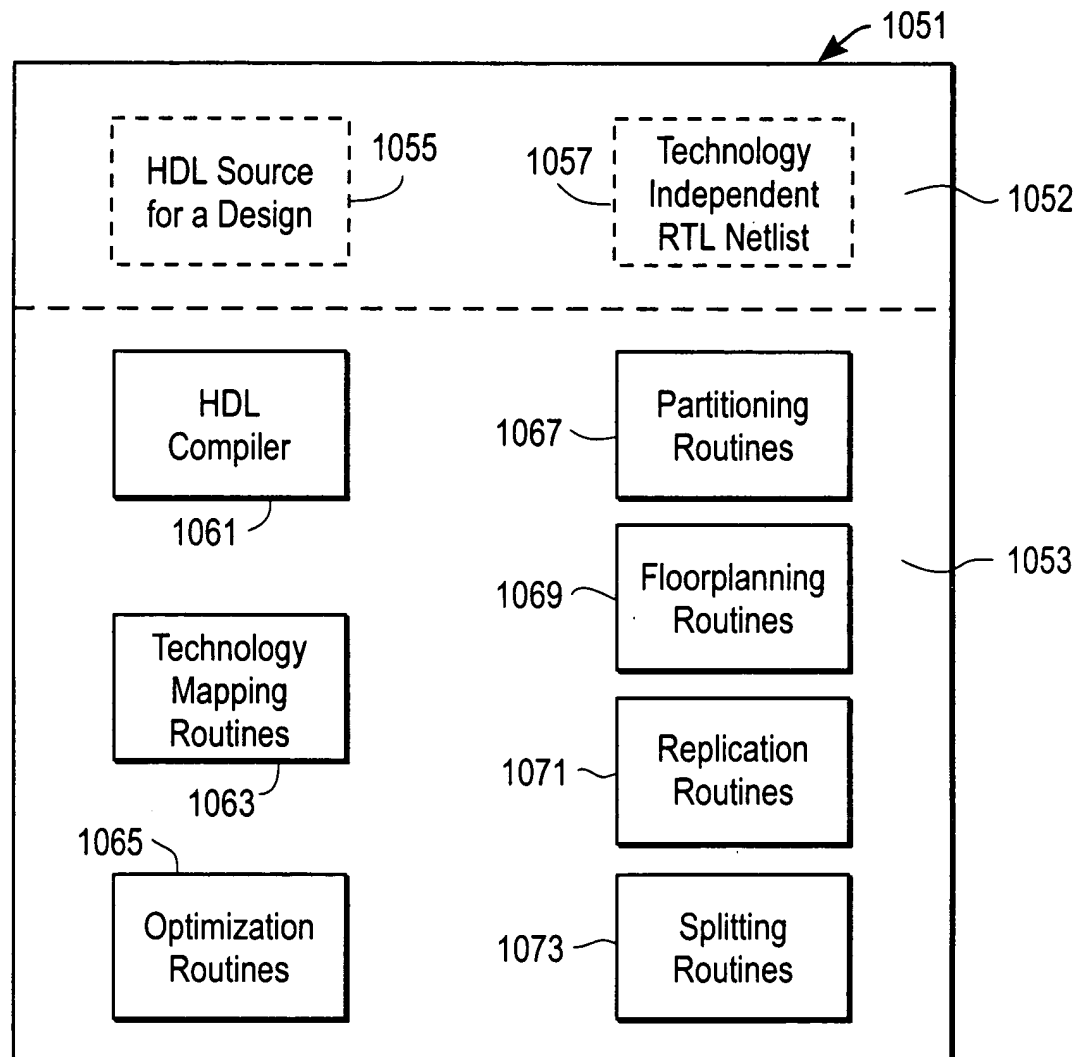


FIG. 13